CLAIM LISTING:

1 - 6. (Currently Cancelled)

7. (Currently Amended) A MOS-controllable power semiconductor device for use in an integrated circuit, the device having an active region that includes a drift region, at least a portion of the drift region being provided in a membrane having opposed top and bottom surfaces, at least one electrical terminal connected directly or indirectly to the top surface and at least one electrical terminal connected directly or indirectly to the bottom surface to allow a voltage to be applied vertically across the drift region, the bottom surface of the membrane not having a semiconductor substrate positioned adjacent thereto.

8. (Previously Presented) A device according to claim 7, wherein only part of the drift region is provided in the membrane.

9. (Previously Presented) A device according to claim 7, wherein the whole of the drift region is provided in the membrane.

10. (Previously Presented) A device according to claim 7, comprising at least one isolation layer surrounding the drift region.

11. (Previously Presented) A device according to claim 10, wherein the at least one isolation layer is provided in said membrane or in a separate membrane to extend from the top surface of the membrane to the bottom surface of the membrane.

12. (Previously Presented) A device according to claim 7, comprising at least one isolation layer surrounding the drift region and provided outside the membrane.

13. (Previously Presented) A device according to claim 10, wherein the or at least one isolation layer is provided by electrically insulating material.

14. (Previously Presented) A device according to claim 10, wherein the or at least one isolation layer is provided by a highly doped semiconductor layer which in use is biased to provide a junction that is reverse-biased or biased below the forward-bias level.

15. (Previously Presented) A device according to claim 7, and further comprising at least one additional power device having a drift region at least a portion of which is provided on said membrane or on a separate membrane.

16. (Previously Presented) A device according to claim 7, and further comprising at least one low voltage device.

17. (Previously Presented) A device according to claim 16, wherein said at least one low voltage device is provided in said membrane.

18. (Previously Presented) A device according to claim 16, wherein said at least one low voltage device is provided outside said membrane.

19. (Previously Presented) A device according to claim 18, wherein said at least one low voltage device is provided in a further membrane.

20. (Previously Presented) A device according to claim 15, comprising at least one isolation layer, said isolation layer providing electrical isolation between adjacent devices.

21. (Previously Presented) A device according to claim 20, wherein the said isolation layer is placed on a further membrane.

22. (Previously Presented) A device according to claim 7, comprising an electrically insulating and thermally conductive layer adjacent the bottom surface of the membrane.

23. (Previously Presented) A device according to claim 7, wherein the membrane comprises a semiconductor layer provided on an electrically insulating layer.

24. (Previously Presented) A device according to claim 7, comprising a mechanically strong and electrically insulating layer provided under the membrane.

25. (Previously Presented) A device according to claim 7, wherein the drift region has a non-uniform doping profile.

26. (Previously Presented) A device according to claim 25, wherein the doping concentration of the drift region at a high voltage terminal side of the device is relatively high and the doping concentration of the drift region at a low voltage terminal side of the device is relatively low.

27. (Previously Presented) A device according to claim 25, wherein the doping concentration of the drift region varies linearly from one side of the drift region to the other.

28. (Previously Presented) A device according to claim 7, wherein the drift region comprises at least two semiconductor layers of alternating conductivity type arranged one above the other and in contact with each other.

29. (Previously Presented) A device according to claim 7, wherein the drift region comprises a plurality of laterally adjacent semiconductor regions of alternating conductivity type.

30. (Previously Presented) A device according to claim 7, wherein the drift region comprises a plurality of laterally adjacent semiconductor cells of alternating conductivity type arrayed around the plane of the device.

31. (Previously Presented) A device according to claim 7, comprising a termination region adjacent to and in contact with the drift region, said termination region being provided to reduce the effect of premature breakdown at the edge of the drift region.

32. (Previously Presented) A device according to claim 31, wherein at least a portion of the said termination region is placed inside the membrane.

33. (Previously Presented) A device according to claim 31, wherein at least a portion of the said termination region is placed outside the membrane.

34. (Previously Presented) A device according to claim 31, wherein the drift region is more highly doped than at least a portion of the termination region.

35. (Previously Presented) A device according to claim 31, wherein the drift region is more highly doped than the semiconductor substrate.

36. (Currently Amended) A MOS-controllable power semiconductor device for use in an integrated circuit, the device having an active region that includes a drift region provided in a layer, the layer being provided on a semiconductor substrate, at least a portion of the semiconductor substrate below at least a portion of the drift region being removed such that said at least a portion of the drift region is provided in a membrane defined by that portion of the layer below which the semiconductor substrate has been removed, and at least one electrical terminal connected directly or indirectly to the top surface and at least one electrical terminal connected directly or indirectly to the bottom surface to allow a voltage to be applied vertically across the drift region.

37. (Previously Presented) A device according to claim 36, wherein only part of the drift region is provided in the membrane.

38. (Previously Presented) A device according to claim 36, wherein the whole of the drift region is provided in the membrane.

39. (Previously Presented) A device according to claim 36, comprising at least one isolation layer surrounding the drift region.

40. (Previously Presented) A device according to claim 39, wherein the at least one isolation layer is provided in said membrane or in a separate membrane to extend from the top surface of the membrane to the bottom surface of the membrane.

41. (Previously Presented) A device according to claim 36, comprising at least one isolation layer surrounding the drift region and provided outside the membrane.